Novel dual-V_{th} independent-gate FinFET circuits

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Abstract

This paper describes gate work function and oxide thickness tuning to realize novel circuits using dual-V_{th} independent-gate FinFETs. Dual-V_{th} FinFETs with independent gates enable series and parallel merge transformations in logic gates, realizing compact low power alternatives. Furthermore, they also enable the design of a new class of compact logic gates with higher expressive power and flexibility than conventional forms, e.g., implementing 12 unique Boolean functions using only four transistors. The gates are designed and calibrated using the University of Florida double-gate model into a technology library. Synthesis results for 14 benchmark circuits from the ISCAS and OpenSPARC suites indicate that on average, the enhanced library reduces delay, power, and area by 9%, 21%, and 27%, respectively, over a conventional library designed using FinFETs in 32nm technology.

1. Introduction

The ITRS has proposed multi-gate FETs such as planar double-gate FETs and FinFETs as a possible scaling path for low power digital CMOS technologies [1]. Although early double-gate FETs presented manufacturing challenges associated with vertical structures, more recently, double-gate devices called FinFETs or wrap-around FETs that are compatible with standard CMOS over most of their processing steps have been demonstrated [2]. The channel of a FinFET is a slab (fin) of undoped silicon perpendicular to the substrate. At least two sides of the fin are wrapped around by oxide simultaneously. In this manner, the active regions are broken up into several fins and a gate overlaps the channel regions of the fins on either side. As a result, the increased electrostatic control of the gate over the channel makes very high I_{on}/I_{off} ratios achievable. FinFETs have also shown excellent scalability, suppression of short channel effects, and limited parametric variations.

A FinFET with independent gates is a novel variant of double-gate devices. Two isolated gates are formed by removing the gate regions at the top of the fin. Although the gates are electrically isolated, their electrostatics is highly coupled. The threshold voltage of either of the gates can be easily influenced by applying an appropriate voltage to the other gate. This technology is called multiple independent-gate FET (MIGFET) [3] and can be integrated with regular double-gate devices on the same chip. A successful implementation of a FinFET device with three independent gates has also been reported [4].

Many innovative circuit styles exploiting the extra gate(s) in these devices have been proposed in literature [5–8]. In [5], the authors showed that a pair of parallel transistors in the pull-down or pull-up network of gates can be merged into a single independent-gate FinFET to get a compact low power implementation of the same Boolean function. In [6], four variants for the same function were designed: conventional tied-gate (TG) mode, independent-gate (IG) mode with merged parallel transistors driven by independent inputs, low power (LP) mode with a reverse-biased back-gate, and an IG/LP mode that combined the LP and IG modes. The use of an independent-gate voltage keeper to improve the reliability of dynamic logic has also been proposed in [8]. However, no published work based on FinFETs has explored the possibility of merging series transistors to reduce power and area and/or increase performance.

The first innovation described in this paper is the realization of dual-V_{th} independent-gate FinFETs to enable the merger of pairs of series transistors in logic gates. We show that a dual-V_{th} FinFET can be realized by tuning only the gate work-function and oxide thickness, without any additional biasing scheme. In this manner, new high-V_{th} transistors can be implemented in addition to the regular low-V_{th} ones. These devices will have low resistance only if both independent gates are activated. The high-V_{th} behavior complements the behavior of low-V_{th} independent-gate FinFETs, which have a low resistance when either of the gates is activated. Dual-V_{th} FinFETs with independent gates make it possible to merge series transistors, and simultaneously merging series and parallel devices allows the realization of compact low power logic gates.

The second innovation described in this paper, based on dual-V_{th} FinFETs, is the design of a new class of compact logic gates with higher expressive power and flexibility than conventional forms. It is proposed to use the independent back-gate as an independent input, effectively doubling the number of inputs to a logic gate. Using the rules for static logic, if a high-V_{th} transistor is used in the pull-down network, the corresponding transistor in the pull-up network is a low-V_{th} transistor, and vice versa, respectively. In this manner, it is shown that it is possible to implement 12 unique Boolean functions using only four transistors.

The gates are designed, validated, and calibrated into a technology library using the University of Florida double-gate (UFDG) SPICE model [9]. The UFDG model is a physics-based model that has shown excellent agreement with physical measurements of fabricated FinFETs [9]. It allows several design parameters such as fin width, channel length, gate-source/drain underlap, and work-function to be varied simultaneously. This enables fast, accurate exploration of the best technologically feasible parameters required to realize independent-gate dual-V_{th} FinFETs for the 32 nm node. These FinFETs were used to build basic and novel gates, whose logical effort parameters were extracted into conventional and enhanced technology libraries. Synthesis results for 14 benchmark circuits from the ISCAS and OpenSPARC suites show that on average, the enhanced library reduces delay, power, and area by 9%, 21%, and 27%, respectively, over a conventional library based on tied-gate FinFETs in 32nm technology.

Section 2 is a basic review of FinFETs. Section 3 describes the design of dual-V_{th} independent-gate FinFETs. Section 4 describes new circuit styles based on these FinFETs. Section 5 presents results and section 6 is a conclusion.

The authors would like to acknowledge Leo Mathew at Applied Novel Devices, Austin for helpful discussions and suggestions. This research was supported by NSF CAREER Award CCF-0746850.

978-1-4244-5766-3/10/$26.00 ©2010 IEEE

2. Background on FinFETs

Double-gate devices were first investigated because intuitively an additional gate is expected to suppress short channel effects and improve I_{on}/I_{off} ratios by increasing electrostatic stability. Quantitatively, the electric potential along the undoped channel (x direction) can be approximated by

$$\phi = C_0 \cdot \exp\left(\pm\frac{x}{\lambda}\right)$$

where C_0 is a constant and λ is the natural length of the device. λ, given by the following expression [1]:

$$\lambda = \sqrt{\frac{\varepsilon_{Si}}{n \cdot \varepsilon_{ox}} t_{ox} t_{Si}}$$

should be as small as possible to quickly damp the influence of drain potential on the channel. This is possible by using high-κ dielectric materials, decreasing oxide thickness t_{ox} and/or silicon thickness t_{Si}, or by increasing the relative control of the gate through coefficient n. Here, n is one for single-gate devices and two for double-gate devices. Thus, using double-gate devices not only helps suppress short channel effects, but also relaxes the physical requirements on t_{Si} and t_{ox} .

The channel of a FinFET is a tiny slab (fin) of undoped silicon perpendicular to the substrate. The cross-section of a typical FinFET is presented in Fig. 1. The undoped channel eliminates Coulomb scattering due to impurities, resulting in higher mobility in FinFETs [10]. The ratio of p-type to n-type mobility is higher than CMOS. Unlike CMOS, threshold voltage is not altered by source-body voltage variation. This, along with improvement in mobility, paves the way for longer series stacked transistors in the pull-up or pull-down networks of logic gates. The gate oxide is formed on both sides of the fin simultaneously, which solves alignment issues of source and drain junctions and simplifies the process. The height of the fin, h_{fin}, acts as the width of channel. Stronger devices can be built by using appropriate number of parallel fins in each transistor. So, the channel width of a FinFET is given by $W = n_{fin} \times h_{fin}$, where n_{fin} is the number of fins. Taller fins result in more powerful devices, at the cost of granularity in gate width. Other important design parameters are fin thickness t_{Si} and gate-source/drain underlap. Existence of gate-source/drain underlap and small t_{Si} are necessary conditions for good suppression of short channel effects in FinFETs [11].

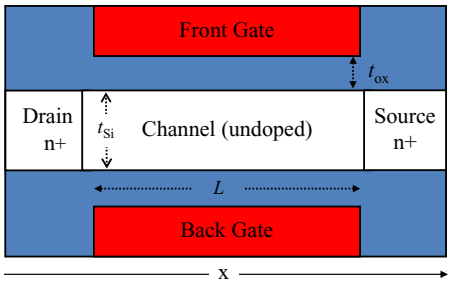

Figure 1: Cross section of a typical FinFET

One of the best available models for FinFETs is the University of Florida Double-gate (UFDG) model. Excellent agreement with physical measurements have been reported for this model [9]. UFDG successfully accounts for quantum mechanical carrier distribution in the body and channel in both the sub-threshold and strong inversion regions of operation. Furthermore, the UFDG model is a physical model that allows designers to change several design parameters such as fin width, channel length, gate-source/drain underlap, and work function simultaneously. All simulations reported in this paper were performed with the UFDG model. In table 2, we report the typical ranges of physical parameters for a 32 nm FinFET technology used in our simulations. Note that all the parameters are in the acceptable range for this technology node.

Table 1: Physical parameters of 32nm FinFETs

Parameter	Range
t_{ox} front	1-2 nm
t_{ox} back	1-2 nm
source/drain doping	(1-2)·10^{20}
work function n-type	4.4-4.85 eV
work function p-type	4.7-4.35 eV
h_{fin}	30 nm
t_{Si}	9 nm
gate-source/drain underlap	2.5 nm

3. Dual-V_{th} independent-gate FinFETs

Independent-gate (IG) FinFETs can be fabricated along with conventional tied-gate (TG) devices on the same die, by removing the top gate region of the FinFET. Channel formation in one gate is highly dependent on the state of the other gate due to electrostatic coupling between the gates. For example, assume that the back-gate of an IG FinFET is disabled. No channel will be formed near the disabled gate and due to electrostatic coupling between the gates, the threshold voltage of the other gate will be increased. So, disabling one of the gates in an IG FinFET will reduce the drive strength of the transistor by more than half. However, it may speed up the circuit indirectly. Disabled gates have an input capacitance that is roughly half that of conventional tied-gate FinFET. This reduces the load on the driver gates, making disabled-gate FinFETs an attractive option for use on non-critical paths in a design.

In conventional IG FinFET devices, a channel will be formed if either of the gates is activated. In other words, the device behaves like the OR function; so, they are suitable for merging parallel transistors in pull-up or pull-down networks. However, in order to merge series transistors, we need devices that behave like the AND function. Such a device would have a higher threshold voltage than regular ones. In these devices, if just one gate is activated, the threshold voltage is high enough to prevent meaningful channel formation. But, if the other gate is also turned on, fast electrostatic coupling between the two gates reduces the threshold voltage and enables channel formation. In other words, these high-V_{th} devices can be activated only if both of their gates are activated simultaneously, so they act like an AND function. Such IG FinFETs are suitable for merging series transistors. Note that high-V_{th} FinFETs cannot be realized by engineering the channel dopant concentration, like [12], because, the FinFET channel should be kept undoped to avoid excessive random dopant fluctuations.

In this paper, we show that high-V_{th} IG FinFETs can be realized by carefully tuning the gate oxide thickness and electrode work-function, and without the use of any additional bias voltages. The threshold voltage V_{th} of FinFETs is given by the expression:

$$V_{th} = -\phi_{ms} + \frac{Q_D}{C_{ox}} + V_{inv} \quad (1)$$

where ϕ_{ms} is the difference between work-function of electrode and silicon, Q_D is the depletion charge in the channel, and C_{ox} is the gate capacitance. V_{inv} is a constant that represents the limited availability of inversion charges in the undoped channel [1]. The thresh-

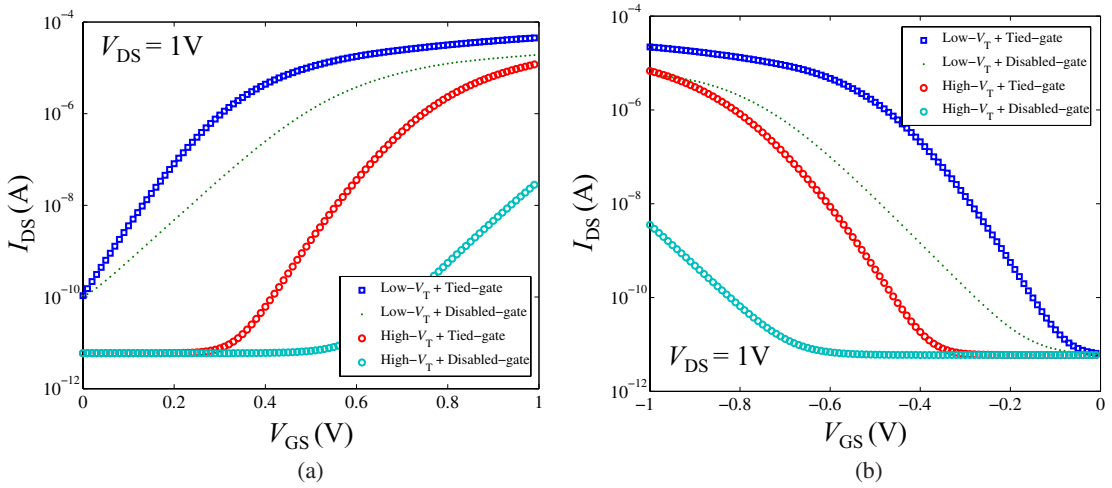

Figure 2: I-V curves of (a) n-type and (b) p-type high-V_{th} and low-V_{th} FinFETs in tied-gate and disabled back-gate modes

old voltage can be increased by changing the gate work-function or decreasing the oxide capacitance (i.e., by increasing t_{ox}). In FinFETs, work-function has much higher impact on threshold voltage than t_{ox} since Q_D is relatively small in undoped or slightly doped channels. In practice, leakage first decreases as oxide thickness is increased. Beyond a certain oxide thickness, however, this trend reverses and standby leakage current increases due to severe DIBL effects. In these undoped devices, the gate loses control over the channel if the oxide thickness is increased aggressively [13]. So, there exists an optimum gate oxide thickness for obtaining minimum leakage. This value was found to be around 2nm for the high-V_{th} 32nm FinFETs considered in this paper.

The oxide thickness and gate work-function of p-type and n-type FinFETs were swept over their ranges in UFDG to obtain the optimum combination of these two parameters. Note that technologically, fabricating multiple work-functions requires two additional steps to mask and etch the gate material. It is also possible to have two values for oxide thickness; even FinFETs with asymmetric back and front gate oxide thickness have recently been reported [14]. SPICE simulations with the UFDG model showed that using the physical parameters in Table 2 results in acceptable performance with minimum static leakage in both high-V_{th} and low-V_{th} devices. I-V curves of n-type and p-type FinFETs for four configurations: low-V_{th} tied-gate, low-V_{th} disabled-gate, high-V_{th} tied-gate and high-V_{th} disabled-gate are shown in Fig. 2.

The threshold voltage can be defined as the intercept of the tangent line of I-V curve and x-axis, at low $V_{DS} \approx 0.05$V [15]. Threshold voltage of both high-V_{th} and low-V_{th} FinFETs in tied-gate (TG) and disabled back-gate modes (IG) are listed in Table 2. As expected, the threshold voltage difference between TG and IG modes is considerably higher in high-V_{th} devices than low-V_{th} devices. In the IG mode of low-V_{th} FinFETs, the inversion layer can be easily formed. This channel shields further gate-to-gate coupling and prevents a huge drop in threshold voltage in the IG mode [12]. In contrast to low-V_{th} devices, no inversion layer can be formed in the IG mode of high-V_{th} FinFETs. Thus, when both gates in a high-V_{th} FinFET are simultaneously on, the strong electrostatic coupling between them creates an inversion layer and produce an acceptable I_{on}.

As seen in Fig 2, the reported static leakage current in UFDG is of the order of a few pA. This is to be expected for well-engineered FinFETs with a t_{si}:L_{ch} ratio of 1:4 and good gate-source/drain underlap. This is also consistent with I_{off} reported for recently manufactured FinFETs [14]. From the I-V curves, it is clear that if just one gate is activated in high-V_{th} transistors, the current is low enough that the transistor can be considered to be in the off-state. So even in this case, these devices will still have low static leakage. In the case of low-V_{th} devices, if just one of the gates is activated, the device can be considered to be in the on-state. However, its current drive is around 60% less than the current drive of tied-gate devices. This makes the gates with merged series or parallel transistors slower than gates with tied-gate transistors and limits their use to non-critical paths. Note that the UFDG model does not model gate leakage, which is expected to be low in FinFETs due to the presence of a low electric field across the gate and sufficient gate-source/drain underlap.

Table 2: V_{th}, t_{ox}, and gate work-function (ϕ) of high-V_{th} (H) and low-V_{th} (L) devices in tied-gate (TG) and disabled back-gate (IG) modes

	t_{ox} (nm)		ϕ (eV)		V_{th} (V)			
					TG		IG	
	L	H	L	H	L	H	L	H
n-type	1	1.9	4.4	4.85	0.18	0.486	0.27	0.77
p-type	1	2	4.7	4.35	-0.2	-0.5	-0.29	-0.79

The proposed high-V_{th} IG devices are robust to parametric variations in oxide thickness and do not lose their AND-type functionality. Variations in oxide thickness degrades subthreshold slope and changes the gate capacitance, but does not have a huge impact on the V_{th} of these devices due to negligible inversion charge Q_D (see Eq. 1). As reported in Table 2, the V_{th} difference between the high and low-V_{th} IG devices is relatively large ($\approx$ 500 mV). Further, FinFETs are known to be less susceptible to parametric variations in comparison to planar CMOS. Thus, the conversion probability of a high-V_{th} device to a low-V_{th} device due to imperfections in the fabrication process is negligible.

Switching characteristics of inverters based on both high-V_{th} and low-V_{th} devices were investigated. Both low-V_{th} and high-V_{th} inverters showed excellent switching behavior and near perfect noise margin (400 mV $\approx 0.5V_{dd}$). In the next section, we describe new circuit styles and logic gates based on these dual-V_{th} FinFETs.

4. Logic design in FinFET technology

In this section, several innovative gate designs based on dual-V_{th} independent-gate FinFETs are described. In the first sub-section, the gates that are created by disabling the back-gate and merging series and parallel transistors are investigated. In the next sub-section, new logic gates that incorporate both low-V_{th} and high-V_{th} devices are described. Complex Boolean functions can be realized efficiently using these devices. To the best of our knowledge, such gates have not been investigated for FinFET technology in literature. The circuit symbols of dual-V_{th} FinFETs in TG and IG configurations are summarized in Fig. 3.

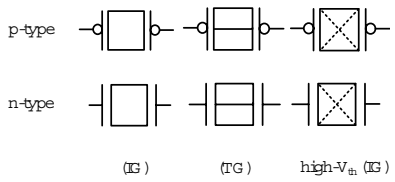

Figure 3: Symbols for independent-gate (IG) and tied-gate (TG) low-V_{th} and high-V_{th} n-type and p-type double-gate FinFETs. The dotted-X sign in high-V_{th} devices denotes their AND-like behavior.

4.1 Merging and back-gate disabling

Without loss of generality, Fig. 4 presents all possible realizations of a NAND2 gate. NAND2 is the conventional gate that uses low-V_{th} FinFETs in tied-gate configuration. NAND2_dis is derived by disabling the back-gates of all devices in the conventional NAND2 gate. NAND2pu is the result of merging two parallel transistors and replacing it by one low-V_{th} FinFET in the pull-up network of NAND2. NAND2pu_dis is derived by disabling the back-gates of pull-down devices of NAND2pu. The two series transistors in the pull-down network of the conventional NAND2 gate can be replaced by one high-V_{th} transistor to realize NAND2pd. NAND2pd_dis is derived by disabling the back-gates of pull-up devices in NAND2pd. Finally, one can merge both series and parallel transistors in the conventional NAND2 gate to realize NAND2pdpu. In Table 3, low-to-high (T_{plh}) and high-to-low (T_{phl}) transition delays, input capacitance (C_{in}) and average static power consumption of these gates are reported. As shown in the table, the gates realized by merging parallel transistors or disabling the back-gate have generally less input capacitance, leakage power, and gate overdrive. So, there exists a tradeoff in choosing the appropriate gates for optimum power and performance.

From the table, it is also seen that merging parallel transistors does not affect static power consumption. However, merging series transistors that requires an independent-gate high-V_{th} FinFET increases static power by roughly two orders of magnitude. This is because for some input patterns, one of the gates of a high-V_{th} FinFET is active while the other gate is inactive. Although the high-V_{th} FinFET is supposed to be in the off-state, the activation of one of its gates reduces the threshold voltage and results in an increase in static power consumption. Since the FinFETs were engineered with adequate gate-source/drain underlap and t_{Si}:L ratios, the leakage current does not exceed 6.4nA, which is comparable to 2.9nA for an equivalent planar 32nm CMOS technology [16].

Both series and parallel merge transformation and back-gate disabling results in a circuit with higher worst-case transition delay. The only exception is the NAND2pu_dis gate, whose worst-case delay is better than the worst-case delay of the NAND2pu gate. This is because although the pull-up network of both gates consists of just one low-V_{th} FinFET, the back-gate of the pull-down transistors are disabled only in NAND2pu_dis. As a result, the T_{plh} and T_{phl} of NAND2pu are not balanced and a race exists between pull-up and pull-down networks while it switches. On the other hand, disabling the back-gate of n-type devices in NAND2pu_dis lessens the drive power of the pull-down network and mitigates this problem [6].

Table 3: Power and delay of conventional and novel gates.

	T_{phl}(ps)	T_{plh}(ps)	I_{off}(pA)	C_{in}(aF)	Number of transistors
NAND2	4.0	4.9	14.6	60.3	4
NAND2_dis	9.4	11.5	13.8	35.4	4
NAND2pu	2.9	10.7	13.0	45.4	3
NAND2pu_dis	10.1	9.6	12.8	41.0	3
NAND2pd	8.6	4.9	6388.7†	45.3	3
NAND2pd_dis	8.4	11.9	6388.0†	32.6	3
NAND2pdpu	7.9	11.0	6378.7†	30.9	2

† Note that the leakage current does not exceed 6.4nA, which is comparable to 2.9nA for an equivalent planar 32nm CMOS technology [16]

4.2 Novel dual-V_{th} logic gates

The availability of dual-V_{th} IG FinFETs motivates design of a new class of compact logic gates with higher expressive power and flexibility. Instead of applying transformations to conventional gates, it is proposed to use the independent back-gate as an independent input, effectively doubling the maximum number of inputs to a logic gate. Both high-V_{th} and low-V_{th} transistors are utilized in both the pull-up and pull-down networks. High-V_{th} independent-gate devices inherently act as an AND function. They will have low resistance if both their inputs are on. So, they can be considered as a network with two series transistors. With the same reasoning, low-V_{th} independent-gate FinFETs can be represented by two parallel transistors in the Boolean network. The rules for static logic require that the pull-down network should be the dual of the pull-up network. Hence, if a high-V_{th} transistor is used in pull-down network with inputs a and b, the corresponding device in the pull-up network is a low-V_{th} device with inputs a and b and vice versa, respectively.

Starting from a structure that resembles the NAND2 gate in Fig. 5, low-V_{th} transistors are used in the pull-down network and high-V_{th} ones in the pull-up network. The stacked devices show higher resistance than parallel ones. So, it is preferable to use the stronger low-V_{th} devices in series structures. It ensures that it is easier to balance pull-up and pull-down networks during design. For the logic gate shown in Fig. 5, the pull-down network will be activated *iff* the Boolean function of Eq. 2 holds.

$$\text{PD} = (a + b) * (c + d) \tag{2}$$

Similarly, the pull-up network will be activated *iff* Eq. 3 holds.

$$\text{PU} = (a^{'} * b^{'}) + (c^{'} * d^{'}) \tag{3}$$

These two equations are Boolean complements and they will never be true simultaneously. So, the logic gate represented in Fig. 5 is a static logic gate. Other compact Boolean functions can be realized from this structure. For example, if c and d inputs are replaced by the complements of inputs a and b, (i.e., $c = a^{'}$ and $d = b^{'}$), the gate becomes one of the most compact implementations of XNOR logic. This structure is flexible and can easily realize the XOR function when b, c and d are replaced with $b^{'}$, $a^{'}$, b. In the first row of Table 4, average leakage, worst case delay, and input capacitance of this gate for different configurations are listed.

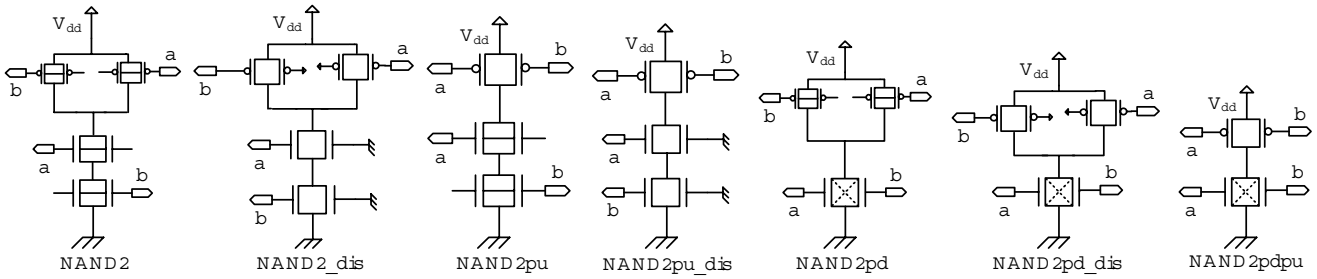

Figure 4: NAND2 gates designed by disabling the back-gates and merging parallel or series transistors

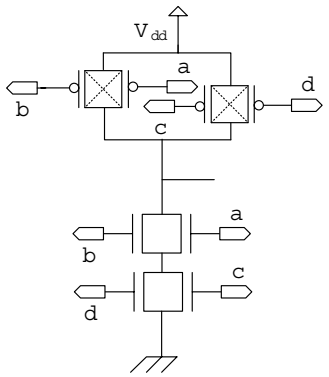

Figure 5: Novel implementation of $[(a+b)*(c+d)]'$

Independent-gate dual-V_{th} FinFETs increase the available options in logic circuit design. For example, it is possible to implement 12 unique Boolean functions using only four transistors as follows. Since the pull-up network is the dual of the pull-down network, it is sufficient to enumerate all the unique configurations in the pull-down network. A logic gate with two IG transistors in the pull-down network can have two, three, or four inputs. With two inputs, all the devices should be TG low-V_{th} devices, i.e., there is only *one* option. With three inputs, one of the FinFETs must be an IG FinFET and the other must be a TG FinFET. *Two* options exist for the IG device: a high-V_{th} or a low-V_{th} device. Finally, with four inputs, all devices must be IG, and *three* possible options exist: both low-V_{th} , both high-V_{th} , and a low-V_{th} along with a high-V_{th} FinFET. Thus, we have six unique combinations of dual-V_{th} FinFETs. Finally, since the two transistors in the pull-down network can be in series or in parallel, a total of twelve unique Boolean functions can be realized using four independent-gate dual-V_{th} FinFETs.

Table 4: Characteristics of selected gates with four transistors

Function	T_{phl}(ps)	T_{plh}(ps)	I_{off}(pA)	C_{in}(aF)
$[(a+b)*(c+d)]'$	12.7	12	1231	38
$[(a*b)*(c*d)]'$	10.0	12.1	3644.8	25.9
$[(a*b)*(c+d)]'$	10.0	12.9	4868.8	28.9
$[(a*b)+(c*d)]'$	10.9	11.1	4790.7	34.2
$[(a*b)+(c+d)]'$	11.1	13.9	1129.2	23.2
$[a+(b*c)]'$	7.3	9.3	3199.6	47.6

Some configurations are not as competitive in performance as other members of this logic family. This is mostly due to a large difference between low-to-high and high-to-low transition delay that occurs when high-V_{th} devices are stacked in either the pull-down or pull-up network. Although it is possible to address this by increasing the width (fin height) of stacked transistors, it will result in a large increase in input capacitance of the gate and keeps the fanout-of-four delay of gate almost unchanged. Performance metrics for the most useful logic gates of this family are listed in Table 4.

The number of logic gates that can be implemented using dual-V_{th} FinFETs has an exponential relationship with the number of transistors in the gate. For example, if the gate has six transistors (three each in the pull-down and pull-up network), 54 unique gates can be realized. Although some of the 54 gates are functionally equivalent, they are structurally different. Further, as illustrated for the case with four transistors, the performance of some gates is not attractive for use in logic circuits. In Table 5, the average leakage, delay, and input capacitance of some of the best gates of this logic family with six transistors is presented.

Table 5: Characteristics of selected gates with six transistors

Logic	T_{phl}(ps)	T_{plh}(ps)	I_{off}(pA)	C_{in}(aF)
$[(a+b)*c*d]'$	12.0	12.6	148.8	25.3
$[(a*b)*c*d]'$	12.1	13.1	1585.4	25.4
$[(a+b)*(c+d)*e]'$	13.5	13.3	420.4	26.7
$[(a+b)*(c+d)*(e+f)]'$	14.8	13.8	928.4	28.8
$[(a+b)+c+d]'$	8.7	18.8	141.8	28.7
$[(a*b)+c+d]'$	8.9	17.8	1603.9	23.0
$[(a*b)+(c*d)+e]'$	9.4	19.4	4775.9	24.5
$[(a*b)+(c*d)+(e*f)]'$	9.6	20.1	10692.1	26.6

5. Results

This section presents results for the area and power reduction that the proposed circuit innovations offer, and compares these results to previously published work. In the first step, logical effort [17] parameters of all novel and conventional gates are extracted using rigorous UFDG SPICE simulations. They consist of input and output capacitances, intrinsic delay, fanout-of-four delay, rise and fall resistance, and static leakage for all input vector permutations. In the next step, four technology libraries are generated using the extracted parameters. They are called basic, previous work, merged series (MS), and complete libraries.

1. Basic library: It is the simplest library and contains only the conventional gates, i.e., tied-gate NOT, NAND2, NOR2, NAND3, NOR3, AND_OR and OR_AND logic.
2. Previous work library: In addition to the gates from the basic library, this library contains the logic gates that are realized by merging parallel transistors or disabling the back-gate as proposed in prior work [5, 6].
3. Merged series library (MS): The MS library uses high-V_{th} devices along with regular low-V_{th} devices, and contains all the gates that are realized by merge series transformation. MS is a super-set of the two previous libraries, but excludes the novel logic gates.

Table 6: Static and dynamic power, area, and delay for benchmark circuits from the ISCAS and SPARC benchmarks, mapped using four different technology libraries. Static power (Stat) is in nW, dynamic power (Dyn) is in mW, area (Area) is reported as the number of fins, and delay (Delay) is in ps. Dynamic power of a circuit is estimated at 85% of the frequency established by the basic library for that circuit.

Circuit	Basic				Previous work				Merged series				Complete			
	Power		Area	Delay	Power		Area	Delay	Power		Area	Delay	Power		Area	Delay
	Stat	Dyn			Stat	Dyn			Stat†	Dyn			Stat†	Dyn		
b9	8.2	0.33	1676	16	8.31	0.31	1603	15	316	0.31	1407	17	201.2	0.26	1197	18
C880	32.7	0.38	6036	61	30	0.34	5615	59	1158	0.35	5618	60	920	0.28	4329	58
C1908	30.7	47.5	7770	104	25.6	49.0	6674	103	583.0	45.1	5434	100	799.35	36.70	4904	93
C499	33.3	41.5	8530	81	32.5	38.3	8010	83	703.1	38.7	7683	80	851.79	30.44	5862	74
C3540	68.2	112	18670	116	64.9	104.7	17832	114	11998	83.8	12978	127	2502.6	86.8	13155	106
sparc_ifu_errctl	107.4	29.8	20668	34	3000	29.1	20400	35	2873.9	23.8	16151	37	3077.3	19.89	13380	40
tlu_hyperv	135.9	51.9	24042	45	116	44.9	20757	52	4793.6	55.3	25845	38	2682.5	38.89	16637	48
C7552	164.1	137.4	25014	83	1423.6	138.8	25663	81	3469.8	116.9	20743	88	3956.8	113.47	19751	83
sparc_ifu_fcl	133.1	61.6	25880	49	141.7	61.9	26364	48	4868	53	21963	50	5497.6	55.2	23274	43
sparc_exu_ecl	150.8	61.3	29734	43	152.6	61.6	30014	44	4015	49.2	23199	45	4890.1	42.8	19874	45
sparc_ifu_ifqdp	156.9	131	29964	70	154.1	123.9	28497	66	6891	112.4	24111	51	6888.7	94.89	20912	56
sparc_ifu_errdp	247.8	211.3	46188	95	224.9	174.7	37356	90	5002.3	180.5	35922	49	7434	99.8	37131	45
C6288	194.1	1059	54024	319	205.9	1115.9	56932	311	1161	949.0	45476	324	8391.20	847.40	39488	307
sparc_exu_byp	420.7	189.2	72058	53	376.5	179.9	68699	56	13628.9	182.7	67669	46	10919.3	176.83	60703	45

† Note that static power is still at most $\approx$ 2% of total power consumption, even in merged series and complete libraries.

4. Complete library: This library is the complete library that contains all the gates from the previous three libraries and the novel logic gates that were introduced in section 4.2.

Synopsys DC was used to synthesize and map fourteen ISCAS and OpenSPARC benchmarks using these four libraries. The area (number of fins), leakage power, dynamic power and minimum achievable critical path delay are listed in Table 5 for all of the benchmarks. In all the circuits and libraries, the static power is at least two orders of magnitude less than the dynamic power. Even after the addition of novel gates with high-V_{th} devices into the MS and complete library, the static power is less than the dynamic power. This is due to the fact that in well-designed FinFETs, the dominant component of power is dynamic power, and all other contributors of power consumption can be reasonably ignored.

Although these libraries have a hierarchical structure and the complete library is the most complete, the library based on just previous work outperforms the MS library in some cases. This can be attributed to the fact that the synthesizer may sometimes converge to local optima. But the overall trend indicates that the previous-work library provides limited reduction in dynamic power or area. However, the MS and complete library are able to provide larger reductions in dynamic power. Specifically, the inclusion of novel gates in the complete library is the main source of improvement. On average, the complete library reduces delay, power, and area by 9%, 21%, and 27%, respectively, over the basic library based on tied-gate FinFETs in 32nm technology.

6. Conclusions

This paper proposes the design of dual-V_{th} independent-gate FinFETs by tuning the oxide thickness and gate work-function. It was shown that the dual-V_{th} independent-gate FinFETs enable merging of series and parallel transistors, enabling efficient realization of logic gates. More complex functions were also designed using dual-V_{th} independent-gate devices in pull-down or pull-up networks of gates. It was shown that significant savings in area and power consumption can be achieved by incorporating these gates into the technology library.

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